

METHODS AND CIRCUITRY FOR IMPLEMENTING FIRST-IN FIRST-OUT  
STRUCTURE

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CROSS-REFERENCE TO RELATED APPLICATION(S)

This application is a continuation of Application No. 09/956,374, filed September 17, 2001, the disclosure of which is incorporated herein by reference.

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FIELD OF THE INVENTION

The present invention relates in general to integrated circuits, and in particular to method and circuitry for implementing high speed first-in-first-out (FIFO) structures.

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BACKGROUND

FIFOs are used in a variety of circuit applications. For example, data communication circuits use FIFO structures to address different system timing requirements. A serializer, for example, employs an internal clock that may not be synchronized with an external clock used to supply data to the circuit. A FIFO is used to transfer the data from the external clock regime to the internal clock regime. Typically, such a FIFO includes a number of registers that operate in response to a write pointer and a read pointer. An external clock usually provides or controls the write pointer while an internal clock controls the read pointer. Even though the phase relationship between these two clock domains is arbitrary, conventional FIFO designs require the frequencies of the two clock signals to be the same. There are applications, however, that require one clock domain to be of different frequency compared to the other (e.g., the write clock frequency be half that of the read clock, or vice versa). Furthermore, FIFOs require additional control

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5           circuitry to ensure the correct timing relationship between  
the write pointers and the read pointers. For example, the  
FIFO pointers must be set to the correct initial positions  
upon start-up, and then reset when any one of a number of  
conditions occur (e.g., overflow, loss of write clock, etc.).  
10          Also, FIFO pointers need to be monitored for a number of  
different purposes including detection of overflow conditions,  
detection of loss of external (write) clock, abnormalities in  
pointer operation, etc.

15          There is a need for improved method and circuitry for  
implementing high speed FIFO structures that meet all of the  
above requirements.

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SUMMARY

20          The present invention provides methods and circuitry for  
implementing high speed FIFO structures. In one embodiment, a  
FIFO is disclosed that allows the frequency of one clock,  
e.g., the write clock, to be different than (e.g., half) that  
of the other (read) clock. In another embodiment a FIFO is  
25          presented that can be set and/or reset asynchronously. Other  
embodiments are disclosed wherein the read and write pointers  
are effectively monitored to ensure proper timing  
relationship, to detect loss of clock as well as to detect  
other abnormal FIFO conditions.

30          Accordingly, in one embodiment, the present invention  
provides a FIFO that includes a plurality of registers; a  
write pointer circuit having an input that receives a write  
clock signal and a plurality of outputs that respectively  
couple to the plurality of registers, the write pointer  
circuit generates a write pointer signal at a first frequency;  
and a read pointer circuit having an input that receives a  
read clock signal and a plurality of outputs that respectively

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5       couple to the plurality of registers, the read pointer circuit  
10      generates a read pointer signal at a second frequency that is  
15      different than the first frequency. In a specific embodiment,  
20      the frequency of the write pointer signal is half of the  
25      frequency of the read pointer signal. In another embodiment,  
30      the FIFO further includes a programming circuit that is  
35      configured to programmably vary the frequency of the write  
40      pointer signal.

In another embodiment the present invention provides a method of operating a FIFO pointer circuit that includes coupling a plurality of shift registers in a circular fashion; and applying a rising edge and a falling edge of a pointer clock signal to clock inputs of the plurality of shift registers in an alternating fashion.

In a further embodiment, the present invention provides a FIFO pointer reset circuit that includes a clock present detector coupled to receive a read clock and a write clock and configured to generate a CKPRES signal indicating status of the write clock; and logic circuit coupled to receive a reset signal, the CKPRES signal, the write clock and the read clock, and configured to generate a write pointer reset signal and a read pointer reset signal in response thereto. More specifically, the logic circuit further receives a lock detect signal indicating phase status of the read clock, the lock detect signal being logically combined with other input signals to the logic circuit. The FIFO pointer reset circuit generates the write pointer reset signal and the read pointer reset signal to respectively reset a write pointer circuit and read pointer circuit when the CKPRES signal indicates loss of the write clock, or when the reset signal is asserted, or when the lock detect signal indicates a no-lock condition for the read clock.

In yet another embodiment, the present invention provides  
5       a method of resetting FIFO pointer circuits that includes  
detecting the presence of a write clock signal and generating  
a CKPRES signal; detecting the lock status of a read clock  
signal phase-locked loop and generating a LCKDET signal;  
receiving a reset signal; and logically combining the CKPRES,  
10      the LCKDET and the reset signal to reset the FIFO pointer  
circuits when the write clock signal is lost, or when the read  
clock is not locked, or when the reset signal is asserted.

In another embodiment, the present invention provides a  
write clock present detector for a FIFO circuit, the write  
clock present detector includes a read shift register having a  
15     first plurality of serially-coupled registers and configured  
to shift a read flag signal in response to a read clock; a  
write shift register having a second plurality of serially-  
coupled register and configured to shift a write flag signal  
in response to a write clock; and a logic circuit coupled to  
20     an output of the read shift register and an output of the  
write shift register, and configured to logically combine the  
write flag signal with the read flag signal to generate a  
write clock present detect output signal. In a specific  
embodiment, the first plurality of registers in the read shift  
25     register is larger in number compared to the second plurality  
of register in the write shift register.

In a further embodiment, the present invention provides a  
method of detecting the presence of a write clock for a FIFO  
circuit, the method including propagating a read flag signal  
30     through a read shift register in response to a read clock;  
propagating a write flag signal through a write shift register  
in response to the write clock; and comparing an output of the  
read shift register with an output of the write shift register  
to generate a write clock present output signal.

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In another embodiment, the present invention provides a  
5       FIFO pointer circuit including a serial chain of N registers  
coupled in circle and configured to shift a pointer signal in  
response to a pointer clock; and a pointer malfunction  
detector having a logic circuit with N inputs respectively  
coupled to N outputs of the N registers, wherein, the logic  
circuit is configured to detect lack of the pointer signal or  
10      presence of multiple pointer signals.

The following detailed description and the accompanying  
drawings provide a better understanding of the nature and  
advantages of the FIFO circuitry according to the present  
invention.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a simplified high-level block diagram of an  
exemplary five-register-deep FIFO circuit;

20      Figure 2 shows a FIFO pointer circuit that operates at  
half the speed of the pointer clock according to one  
embodiment of the present invention;

25      Figure 3 shows a FIFO pointer circuit that can  
programmably operate at either half rate or full rate of the  
clock according to another embodiment of the present  
invention;

Figure 4 shows the FIFO pointer circuit of Figure 3 with  
additional delay matching circuitry according to an  
alternative embodiment of the present invention;

30      Figure 5 shows a FIFO pointer reset circuit according to  
an exemplary embodiment of the present invention;

Figure 6 shows an alternative embodiment for the FIFO  
pointer reset circuit of the exemplary circuit of Figure 5;

35      Figure 7 shows an exemplary circuit implementation for a  
clock present detector according to the present invention; and

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5                  Figure 8 shows an exemplary implementation for a pointer abnormality detector according to another embodiment of the present invention.

DETAILED DESCRIPTION

10                 With reference to the drawings various exemplary embodiments of the present invention will now be described in greater detail.

**FIFO Pointer:**

15                 Referring to Figure 1, there is shown a simplified high-level block diagram of an exemplary five-register-deep FIFO circuit 100. FIFO circuit 100 includes a set of five registers 102-1 to 102-5. It is to be understood that the FIFO of the present invention can have as many stages as desired, and that the 5-stage implementation is described herein for illustrative purposes only. Each of the registers 20       102-1 to 102-5 receives a data input DIN clocked in by respective write pointer signals WPR1 to WPR5. For illustrative purposes, write pointer signals WPR1 to WPR5 are shown as controlling pass switches WrS1 to WrS5, respectively. While this shows a logical depiction of the input circuit, 25       signals WPR1 to WPR5 may be directly applied to clock inputs of registers 102 that may be implemented using, for example, D-type flip flops. The DIN signal would then directly couple to the D input of each register 102. In this embodiment, each register is updated at the falling edge of the corresponding 30       write pointer signal (WPR1-5). The outputs of registers 102-1 to 102-5 connect to a data output node DOUT via read switches RdS1 to RdS5, respectively. Read switches RdS1 to RdS5 are controlled by read clock pointer signals R1 to R5, respectively. FIFO circuit 100 also includes a final register 35

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104 that receives DOUT at its input. Register 104 operates to  
5 synchronize the timing of the signal on DOUT using the read  
clock RCK. FIFO circuit 100 further includes a write pointer  
circuit 106 that generates the write pointer signals WPR1-5 in  
response to write clock WCK. A read pointer circuit 108  
generates read pointer signals RPR1-5 in response to read  
10 clock RCK. A FIFO pointer control circuit 110 receives  
certain control signals such as lock detect LCKDET and pointer  
reset RSTB, as well as write clock WCK and read clock RCK  
signals, and generates control signals for write pointer  
circuit 106 and read pointer circuit 108.

15       In operation, FIFO 100 translates the timing of the input  
data DIN from an external write clock WCK, which controls  
write pointer signals WPR1 to WPR5, to the internal read clock  
RCK, which controls read pointer signals RPR1 to RPR5. In  
most circuit applications read clock RCK and write clock WCK  
have the same frequency. There are applications wherein the  
20      input clock and the output clock may have different  
frequencies. For example, transceiver circuits developed for  
synchronous optical network (SONET) applications, are subject  
to standards set by the Multi-Source Agreement (MSA). In one  
specific application, this standard requires the transceiver  
25      to be able to operate with either a 311MHz input clock or a  
622MHz input clock, and a 622MHz output clock. Therefore, for  
a FIFO used in such a device, the conventional pointer circuit  
design would not satisfy this requirement.

30       Figure 2 shows an exemplary pointer circuit 200,  
according to the present invention, that operates with both  
(falling and rising) edges of the input clock. Pointer  
circuit 200 includes a chain of N clocked registers or flip-  
flops 202-1 to 202-n that are serially connected with the  
output of the last one connecting to the input of the first

one to form a ring. In this exemplary implementation, all flip-flops 202 have an active-low reset input RB except for 5 the first flip-flop 202-1 that has an active-low set input SB. Thus, when a reset signal RSTB is applied to all of flip-flops 202, the outputs P2 through Pn of flip-flops 202-2 to 202-n are reset to logic low or "0", and output P1 of flip-flop 202-1 is set to a logic high or "1". Once the reset signal is 10 removed (e.g., RSTB = "1"), the logic "1" pointer signal shifts through the chain of flip-flops in response to a clock signal CLK. However, instead of directly applying input clock signal CLK to the clock input of each flip-flop 202, the circuit inverts clock signal CLK for every other flip-flop. 15 Thus, given, for example, falling-edge triggered flip-flops 202, it takes two falling edges of the full-rate clock for the logic "1" pointer signal to propagate through one flip-flop 202. In this fashion the pointer circuit operates at half rate clock. The pointer circuit of Figure 2 can be used as 20 the write pointer circuit 106 in Figure 1 for those applications where the input data is received at half the rate of the internal read clock.

To provide the option of operating the pointer circuit at either half rate or full rate, as some applications may 25 require, the present invention provides an alternative embodiment for a dual rate pointer circuit shown in Figure 3. Pointer circuit 300 is similar in its construction to pointer circuit 200 with one modification. For those flip-flops that receive an inverted clock signal, the circuit adds a 30 multiplexer that allows selection between an inverted clock signal or the non-inverted clock signal. Referring to Figure 3, flip-flop 302-2 has its clock input CK2 connected to an output of multiplexer M2. Multiplexer M2 is a 2:1 selection circuit that receives CLK at one input and an inverted version

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of CLK (CLKB) at another. By applying a logic signal to the  
5 select input SEL of multiplexer M2, one of either CLK or CLKB  
is selected to drive the clock input CK2 of flip-flop 202-2.  
Thus, when full rate operation is required, SEL is set to a  
10 logic level that connects the output of multiplexers M2 to  
CLK. This results in all flip-flops 302 simultaneously  
receiving the same edge of CLK. On the other hand, when half  
rate operation is desired, SEL is set to a logic level that  
connects CLKB to the output of multiplexer M2. This results  
15 in half of the flip-flops receiving CLKB with the other half  
receiving KLB at their clock inputs, reducing the frequency of  
operation by half.

15      The inclusion of multiplexers at the clock input of one  
half of the flip-flops and not the other half, introduce delay  
mismatches that may adversely impact the operation of the  
20 circuit. Figure 4 shows an alternative embodiment of a  
pointer circuit 400 wherein dummy multiplexers DM<sub>i</sub> have been  
inserted along the clock path of that half of the flip-flops  
that otherwise received CLK. signal directly. For each dummy  
multiplexer, both inputs connect together and to CLK and the  
25 SEL input is permanently tied to the logic signal that passes  
CLK to the clock input of the respective flip-flop. The  
purpose of the dummy multiplexers is to replicate the delay  
the circuitry introduces in order to match the delay along  
each individual clock line.

30      It is to be understood that the specific pointer circuits  
shown in Figures 2, 3 and 4 are exemplary and for illustrative  
purposes only, and that many variations will be known to those  
skilled in the art. For example, the logic polarities used in  
the various circuits such as set and reset inputs of the flip-  
flops or falling-edge versus rising-edge triggered nature of  
the flip flops, can be readily inverted with known circuit  
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5       techniques. Furthermore, while the various embodiments shown  
10      provide half rate and dual rate pointer circuitry, similar  
15      principals can be used to provide further variations in the  
20      rate of operation. For example, instead of receiving an  
25      inverted version of the clock signal, the multiplexers can  
30      receive a signal that is  $\frac{1}{4}$  of clock signal CLK or any other  
35      fraction thereof. Multiplexers performing 3:1, 4:1 or higher  
40      can be used to provide for selection of multiple rates of  
45      operation. Also, the number of flip-flops that receive a  
50      different clock signal need not be half the total, and any  
55      combination can be used to achieve a desired rate of  
60      operation.

15      To ensure proper operation of a FIFO, not only do the  
20      individual pointer circuits must operate properly, correct  
25      timing relationship between the write pointer and the read  
30      pointer is essential. Referring back to Figure 1, FIFO 100  
35      includes a FIFO pointer control circuit 110 for providing the  
40      control functions that ensure proper operation of the FIFO.  
45      One function performed by control circuit 110 is the setting  
50      (or resetting) of FIFO pointers at the right position when  
55      necessary. For example, when the circuit is first powered up,  
60      read and write pointer circuits must first be reset to the  
65      correct start-up position. A reset may also be necessary  
70      during the operation of the FIFO when, for example, the  
75      external clock is for some reason lost. Depending on the  
80      application of the FIFO circuit other conditions may exist  
85      under which the pointer circuits may require resetting.

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**FIFO Reset:**

Figure 5 shows a specific circuit implementation for an exemplary FIFO reset circuit 500. In this example, it is assumed that there are three control signals. The first is an

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external active-low reset control signal RSTB that may be, for example, under the control of the user. A second control  
5       signal is a lock detect signal LCKDET that indicates successful locking of a phase-locked loop (not shown) that is employed to reproduce a clean internal version of the external clock. A third control signal CKPRES is generated by a clock present detector 502 and detects when the external (write) 10      clock is lost. Each of these control signals give rise to a condition that requires the resetting of the write pointer and the read pointer. To accomplish this, the circuit includes a clock present detector 502 that receives the external write clock WCK and read RCK as inputs and generates control signal 15      CKPRES at an output. An exemplary implementation for clock present detector 502 is shown in Figure 7 and described in greater detail below. An AND gate 504 receives signals CKPRES and LCKDET at its inputs and generates an output signal HOLD. Reset circuit 500 also includes a first flip-flop 506 that 20      receives the external reset signal RSTB at its input and receives the signal HOLD at an active-low reset input RB. Flip-flop 506 is clocked by write clock WCK. Flip-flop 506 thus operates to align external control signal RSTB to on-chip 25      write clock. The read pointer reset is accomplished by a serially-coupled pair of flip-flops 508 and 510. Flip-flop 508 receives the output of flip-flop 506 at its D input, read 30      clock RCK at its clock input, and HOLD signal at its RB input. Flip-flop 510 receives the output of flip-flop 508 at its input, read clock RCK at its clock input and HOLD at its RB input. A pair of inverters buffer the output of flip-flop 510 and generate an active-low read pointer reset signal RRSTB. The write pointer reset signal WRSTB includes a pair of 35      serially-coupled flip-flops 516 and 518, followed by inverters 520 and 422 connected in a similar fashion to the read path.

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FIFO pointer reset circuit 500 is designed to reset the  
read and write pointer circuits when any one of the three  
5 following conditions occurs: (1) when the external write clock  
is lost ( $CKPRES = "0"$ ); (2) when the phase-locked loop has not  
achieved a lock condition ( $LCKDET = "0"$ ); and (3) when the  
external reset signal RSTB forces a reset condition ( $RSTB =$   
10        $"0"$ ). In operation, a logic low at either LCKDET or CKPRES  
causes HOLD to go low resetting each of the flip-flops in  
reset circuit 500. A logic low received at the external reset  
signal RSTB also resets the outputs of all flip-flops within,  
e.g., two to three clock cycles. The external reset control  
provides the user with additional flexibility to ensure  
15       optimized timing. Because the read and write clock signals  
are not in phase, two serially-connected flip-flops 508 and  
510 in the read path are used to ensure that meta-stable  
conditions are avoided. Serially-coupled flip-flops 516 and  
518 in the write path are included to match the delay of their  
20       read path counterparts. Signals RRSTB and WRSTB are applied  
to the reset inputs of the chain of flip-flops in the FIFO  
pointer circuit (see, e.g., Figures 2, 3 or 4). Accordingly,  
when asserted RRSTB and WRSTB release the FIFO pointers from  
the correct starting position. The releasing of the read  
25       pointer is synchronized with read clock RCK, while the  
releasing of the write pointer is synchronized with write  
clock WCK. It is to be understood that Figure 5 provides but  
one exemplary implementation of reset circuitry and that  
variations are possible. For example, signal RSTB need not  
30       necessarily be an external signal and could be generated on-  
chip from other circuitry such as a FIFO overflow detector  
that may require the resetting of the FIFO pointers when  
specific conditions occur.

Figure 6 shows an alternative implementation for the pointer reset circuit that accommodates dual rate pointer circuits and shows other possible modifications. As the circuit of Figure 6 is very similar to that shown in Figure 5, the same reference numerals are used to refer to the same components. Pointer reset circuit 600 of Figure 6 differs from that shown in Figure 5 in that it can handle a dual rate read clock. A D-type flip-flop 602 has its QB output fed back to its D input to form a divide-by-two circuit. Flip-flop 602 receives read clock RCK at its clock input and divides the frequency by half to generate RCKDIV2. A 2:1 multiplexer 604 receives read clock RCK at one input and RCKDIV2 at another. A select input SEL selectively applies either RCK or RCKDIV2 to one input of clock present detector 502. Clock present detector 502 generates signal CKPRES, and AND gate 504 generates signal HOLD in the same fashion as in the circuit of Figure 5. Another 2:1 multiplexer 606 connects at the clock input of flip-flop 516 in the write reset path. Multiplexer 606 allows for programmable selection between the falling edge and the rising edge of write clock signal WCK. In the same manner as in the dual rate FIFO pointer circuit shown in Figure 3, the addition of this multiplexer reduces by half the frequency the reset signal at the output of flip-flop 506 is propagated through flip-flops 516 and 518. Similar to the circuit shown in Figure 4, a dummy multiplexer (not shown) can be used at the clock input of flip-flop 518 to match delays.

In this embodiment of pointer reset circuit 600, along the read path a third flip-flop 612 is added that can be multiplexed in by multiplexer 610. As connected, when the A input of multiplexer 610 is selected the read path will operate with the two flip-flops 508 and 510 (as in the circuit of Figure 5). When the B input of multiplexer 610 is

5           selected, flip-flop 612 is inserted in series with the other  
two flip-flops. The option of adding an extra flip-flop  
enables the circuit to provide different delays in the read  
pointer reset path. This option allows the user to optimize  
alignment of read pointer reset signal RRSTB and write pointer  
reset signal WRSTB.

10          Clock Present Detector:

In another embodiment, the present invention provides an implementation for a clock present detector that can be used in, for example, the FIFO pointer circuits of the type shown in Figures 5 and 6. Figure 7 shows one exemplary circuit implementation for a clock present detector 700. In this embodiment, read clock RCK is an internal signal that may be generated by a phase-locked loop, and is therefore always present. Read clock RCK is used to detect whether an external write clock WCK is or is not present. Detector 700 includes a read chain of serially-connected flip-flops and a write chain of serially-connected flip-flops. In the example shown, the write chain includes three D-type flip-flops 702, 704 and 706, with the first flip-flop (702) having its input connected to a logic high signal, such as the power supply voltage VDD. Write clock WCK is applied to the clock inputs of flip-flops 702, 704 and 706, the output of which is node W1. The read chain includes a similar set of three flip-flops 708, 710 and 712, with the first flip-flop (708) having its input connected to VDD, and all three receiving read clock RCK at their clock inputs. The output of flip-flop 712 is node R1. The read chain includes an additional set of three serially-connected flip-flops 714, 716 and 718 that connect in series with the first set of three flip-flops at node R1. The signals at nodes W1 and R1 are applied to an AND gate 720 the output of

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5       which, node CKDET, is applied to the D input of an output  
flip-flop 722. The clock input of output flip-flop 718  
receives the output of the final flip-flop 718, node R2. A  
reset circuit 724 includes a couple of flip-flops 726 and 728  
connected to the read chain with their outputs connected to a  
NOR gate 730. Reset circuit 724 generates a reset signal  
RESET for the flip-flops in the read and write chain.

10      In operation, the logic "1" at the input of flip-flop 708  
is propagated through the read chain of flip-flops by read  
clock RCK. The logic "1" at the input of flip-flop 702 is  
propagated through the write chain of flip-flops by write  
clock WCK, assuming WCK is present. If write clock is  
15     present, after three cycles the write "1" reaches node W1 and  
waits until the read "1" reaches node R1. Once both R1 and W1  
are asserted, AND gate 720 asserts node CKDET. The logic high  
CKDET remains at the D input of flip-flop 722 until the read  
"1" propagates through the three additional read flip-flops  
20     714, 716 and 718. Once the read "1" reaches node R2, flip-  
flop 722 is clocked responding to its input CKDET. The output  
of flip-flop 722 thus goes high (WCKPRES = "1") signaling the  
presence of the write clock. The purpose of the three  
additional flip-flops in the read chain is thus to provide  
25     some margin (in this example three read clock cycles) before  
WCKPRES signals the presence of clock. When there is no write  
clock signal present, the write "1" does not get propagated  
through the write chain of flip-flops and therefore node W1 is  
not asserted. This keeps CKDET low which in turn keeps  
30     WCKPRES low, signaling the lack of a write clock signal. To  
perform a continuous monitoring of the status of the write  
clock signal, this circuit is reset periodically. The reset  
occurs after the read "1" reaches node R2. One read clock  
cycle thereafter, the output of flip-flop 726 goes high

causing RESET to go low. RESET is applied to the active-low  
5       reset input RB of all of the flip-flops in both the read chain  
and the write chain. Thus, when RESET goes low, the entire  
circuit is reset except for WCKPRES. The state of WCKPRES  
will change to low only if by the time the read "1" reaches  
R2, CKDET is still in a reset state. Such a condition would  
indicate that a previously present WCK signal has been lost.

10      It is to be understood that the specific implementation  
shown in Figure 7 is for illustrative purposes only and that  
many variations for implementing this type of clock present  
detector are possible. For example, the number of flip-flops  
in each chain is arbitrary and is usually arrived at by a  
15     trade off between speed and accuracy. Similarly the number of  
additional flip-flops in the read chain is also arbitrary and  
may change depending on the circuit requirements. For  
example, the exemplary circuit of figure 7 shows a write chain  
that has one half as many flip-flops as the read chain. This  
20     number may be suitable for a FIFO pointer circuit that  
operates at full rate. For a half rate FIFO pointer circuit,  
circuit 700 may be designed with a write chain having one  
quarter as many flip-flops as the read chain. Thus the  
absolute and relative numbers of flip-flops depends on a  
25     number of different factors, including desired speed of  
operation, desired margin allowed for signaling detection,  
FIFO pointer circuit rate of operation, etc.

**FIFO Pointer Abnormality Detector:**

30      Another control function performed by FIFO pointer  
control circuit 110 of Figure 1 is the monitoring of the FIFO  
pointer operation. As discussed above in connection with  
Figures 2, 3 and 4, a FIFO pointer circuit propagates a  
pointer flag (e.g., a logic "1" signal) through a ring of  
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5                  serially-connected flip-flops. Thus the pointer circuit  
any of the flip-flops, or when there are more than one flags  
present. Such abnormal conditions may be caused by glitches  
or clock jitter and the like. In another embodiment the  
present invention provides a circuit that simultaneously  
checks for both of these conditions.

10                 Referring to Figure 8, there is shown an exemplary  
implementation for a pointer abnormality detector 800.  
Circuit 800 includes a large OR gate 802 that receives all but  
one of the outputs of the flip-flops in the pointer circuit.  
Using the pointer circuit shown in any of the Figures 2, 3, or  
15                 4, outputs P<sub>1</sub> through P<sub>(n-1)</sub> may all be respectively applied  
to (n-1) inputs of OR gate 802. The output of OR gate 802,  
node N<sub>1</sub>, connects to one input of an exclusive NOR gate 804.  
The other input of exclusive NOR gate 804 receives the only  
other pointer output P<sub>(n)</sub> that was not connected to OR gate  
20                 802. The output of exclusive NOR gate 804, node N<sub>2</sub>, connects  
to the D input of flip-flop 806. The clock input of flip-flop  
806 is clocked by, for example, a derivative of the read or  
write clock for each pointer circuit, respectively. Thus, if  
25                 there is a malfunction of the type where no pointer flag is  
present (i.e., all pointer flip-flops have a logic "0" at  
their outputs), the output of OR gate 802 would be at a logic  
low (i.e., N<sub>1</sub> = "0"). Because node P<sub>(n)</sub> would also be low,  
the output of exclusive NOR gate 804 would be asserted (N<sub>2</sub> =  
"1"). Once clocked by CK, the output of flip-flop 806 would  
30                 also be asserted resulting in BADPTR = "1" which signals a  
"bad pointer" condition.

For the case where there may be more than one flag  
propagating through the pointer flip-flops, the output of OR  
gate 802 would be high (N<sub>1</sub> = "1") due to one of the logic high

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5       flags.  $P(n)$  however may remain low as long as the one or more additional (errant) flags are among those that connect to the inputs of OR gate 802 (i.e.,  $P_1$  to  $P[n-1]$ ). But as the pointer flags propagate through the pointer circuit flip-flop chain in response to the clock signal,  $P(n)$  will eventually be asserted causing node N2 to go high. This in turn causes BADPTR to go high once flip-flop 808 is clocked. In this fashion, circuit 800 is able to detect both error conditions; the no pointer condition and the multiple pointer condition. Once again, the specific circuit shown in Figure 8 is for illustrative purposes only, and variations are possible. For example, the one pointer output that is selected to directly connect to the exclusive NOR gate need not be the  $n$ th pointer and can be any one of the pointer outputs  $P_1$  to  $P(n)$ . Also, whether an OR gate or an AND gate or any other type of logic gate is used for gate 802 may vary depending on the logic polarity of its input and the type of logic gate connected at 10 its output. The same applies to the other logic gates including exclusive NOR gate 804, AND gate 812 and OR gate 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 1225 1230 1235 1240 1245 1250 1255 1260 1265 1270 1275 1280 1285 1290 1295 1300 1305 1310 1315 1320 1325 1330 1335 1340 1345 1350 1355 1360 1365 1370 1375 1380 1385 1390 1395 1400 1405 1410 1415 1420 1425 1430 1435 1440 1445 1450 1455 1460 1465 1470 1475 1480 1485 1490 1495 1500 1505 1510 1515 1520 1525 1530 1535 1540 1545 1550 1555 1560 1565 1570 1575 1580 1585 1590 1595 1600 1605 1610 1615 1620 1625 1630 1635 1640 1645 1650 1655 1660 1665 1670 1675 1680 1685 1690 1695 1700 1705 1710 1715 1720 1725 1730 1735 1740 1745 1750 1755 1760 1765 1770 1775 1780 1785 1790 1795 1800 1805 1810 1815 1820 1825 1830 1835 1840 1845 1850 1855 1860 1865 1870 1875 1880 1885 1890 1895 1900 1905 1910 1915 1920 1925 1930 1935 1940 1945 1950 1955 1960 1965 1970 1975 1980 1985 1990 1995 2000 2005 2010 2015 2020 2025 2030 2035 2040 2045 2050 2055 2060 2065 2070 2075 2080 2085 2090 2095 2100 2105 2110 2115 2120 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8125 8130 8135 8140 8145 8150 8155 8160 8165 8170 8175 8180 8185 8190 8195 8200 8205 8210 8215 8220 8225 8230 8235 8240 8245 8250 8255 8260 8265 8270 8275 8280 8285 8290 8295 8300 8305 8310 8315 8320 8325 8330 8335 8340 8345 8350 8355 8360 8365 8370 8375 8380 8385 8390 8395 8400 8405 8410 8415 8420 8425 8430 8435 8440 8445 8450 8455 8460 8465 8470 8475 8480 8485 8490 8495 8500 8505 8510 8515 8520 8525 8530 8535 8540 8545 8550 8555 8560 8565 8570 8575 8580 8585 8590 8595 8600 8605 8610 8615 8620 8625 8630 8635 8640 8645 8650 8655 8660 8665 8670 8675 8680 8685 8690 8695 8700 8705 8710 8715 8720 8725 8730 8735 8740 8745 8750 8755 8760 8765 8770 8775 8780 8785 8790 8795 8800 8805 8810 8815 8820 8825 8830 8835 8840 8845 8850 8855 8860 8865 8870 8875 8880 8885 8890 8895 8900 8905 8910 8915 8920 8925 8930 8935 8940 8945 8950 8955 8960 8965 8970 8975 8980 8985 8990 8995 9000 9005 9010 9015 9020 9025 9030 9035 9040 9045 9050 9055 9060 9065 9070 9075 9080 9085 9090 9095 9100 9105 9110 9115 9120 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10935 10940 10945 10950 10955 10960 10965 10970 10975 10980 10985 10990 10995 11000 11005 11010 11015 11020 110

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The present invention has thus provided various  
5       embodiments for a number of different circuits used in a FIFO  
structure, as well as methods of operating the same.  
Embodiments for half rate and dual rate FIFO pointers  
circuits, FIFO pointer reset circuits, clock present detector,  
and pointer abnormality detector are among the various  
10      inventions described herein. After reading and understanding  
the present detailed description, many modifications,  
variations, alternatives, and equivalents will be apparent to  
a person skilled in the art and are intended to be within the  
scope of this invention. Therefore, the specific embodiment  
described is not intended to be exhaustive or to limit the  
15      invention, and the invention is intended to be accorded the  
widest scope consistent with the principles and novel features  
disclosed herein, and as defined by the following claims.

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